



MS APPEAL BRIEF - PATENTS  
Docket No.: 0465-0882P  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Jong KIM et al.

Application No.: 10/029,145

Confirmation No.: 005232

Filed: December 28, 2001

Art Unit: 2871

For: LIQUID CRYSTAL DISPLAY DEVICE AND  
METHOD OF MANUFACTURING THE  
SAME

Examiner: Z. Q. Qi

**APPEAL BRIEF TRANSMITTAL FORM**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief on behalf of the Appellants in connection with the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

A Notice of Appeal was filed on November 23, 2005.

☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27.

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☒ Extension of time fee pursuant to 37 C.F.R. §§ 1.17 and 1.136(a) - \$120.00.

Application No.: 10/029,145

Docket No.: 0465-0882P

- ☒ Fee for filing an Appeal Brief - \$500.00 (large entity).
- ☒ Check(s) in the amount of \$620.00 is(are) attached.
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Dated: February 23, 2006

Respectfully submitted,

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PATENT  
0465-0882P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Jong Il KIM et al. Conf. No.: 5232  
Appl. No.: 10/029,145 Group: 2871  
Filed: December 28, 2001 Examiner: Z. QI  
For: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF  
MAKING SAME

**BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

February 23, 2006

Sir:

Appellants hereby appeal from the decision in the final Office Action dated August 24, 2005 finally rejecting claims 1-12, 14-24 and 26-28.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

- I. Real Party In Interest
- II Related Appeals and Interferences
- III. Status of Claims
- IV. Status of Amendments
- V. Summary of Claimed Subject Matter
- VI. Grounds of Rejection to be Reviewed on Appeal
- VII. Argument
- VIII. Claims
- IX. Evidence
- X. Related Proceedings
- Appendix A - Claims

**I. REAL PARTY IN INTEREST**

The real party in interest for this application is LG. Philips LCD Co., Ltd., as evidenced by an Assignment recorded on December 28, 2001 at Reel 012419, Frame 0440.

**II. RELATED APPEALS AND INTERFERENCES**

To the best of Appellants' knowledge, there are no other prior or pending appeals of this application, or patent interference proceedings, or judicial proceedings which may be related to, directly affect, or be directly affected by, or have a bearing on the Board's decision of this Appeal.

**III. STATUS OF CLAIMS**

In the application on appeal, claims 1-12, 14-24 and 26-28 are pending. Claims 1, 8, 17 and 26-28 are independent. Claims 1-12, 14-24 and 26-28 are rejected and are on appeal.

**IV. STATUS OF AMENDMENTS**

The Amendment under 37 CFR 1.111, filed on June 28, 2004, has been entered. The status of the claims is correctly stated in that Amendment.

**V. SUMMARY OF THE CLAIMED SUBJECT MATTER**

Claims 1, 8, 17 and 26-28 are the six independent claims.

Claim 1 is directed to an LCD device comprising (1) a substrate, *e.g.*, 11; (2) a TFT having a gate electrode and source/drain electrodes on the substrate, *e.g.*, as shown in Figs. 3C, 3D, 4C and 4D; (3) a passivation film, *e.g.*, 18, formed on an entire surface of the substrate and having a contact hole in the drain electrode of the TFT; and (4) a pixel electrode, *e.g.*, 19a, made of an amorphous transparent conductive film of sufficient thickness to prevent a generation of a galvanic effect, and connected to the drain electrode through the contact hole, the drain electrode having a single-layer structure.

Claim 8 is directed to a pad structure of an LCD device, comprising (1) a substrate, *e.g.*, 11; (2) a metal film, *e.g.*, 12c, formed on the substrate and functioning as a pad for the LCD device; and (3) an amorphous transparent conductive film, *e.g.*, 19c, of sufficient thickness to prevent a generation of a galvanic effect, and formed on the metal film, wherein the metal film is formed of a same material as a gate line or a data line.

Claim 17 is directed to a method for manufacturing an LCD device, comprising the steps of (1) forming a gate line including a gate electrode and a gate pad on a substrate; (2) forming a gate insulating film on an entire surface of the substrate; (3) forming a semiconductor film above the gate electrode; (4) forming a data line including a data pad to form source and drain electrodes of a TFT at both sides above the semiconductor film; (5) forming a passivation film on the entire surface of the substrate; (6) forming contact holes in the drain electrode, the gate pad and the data pad of the TFT; and (7) forming, in each pixel region, amorphous transparent conductive films of sufficient thickness to prevent a generation of a galvanic effect, and connected to the drain electrode,

the gate pad and the data pad through the contact holes, wherein at least one of the drain electrode, the gate pad and the data pad has a single-layer structure. Appellants respectfully direct the attention of the honorable Board members to Figs, 3A-3D and 4A-4D, which illustrate semiconductor device structures at different stages of the claimed method.

Claim 26 is directed to an LCD device comprising (1) a substrate, *e.g.*, 11; (2) a TFT having a gate electrode and source/drain electrodes on the substrate, shown, for example, on the left side of Figs. 3C, 3D, 4C and 4D; (3) a passivation film, *e.g.*, 18, formed on an entire surface of the substrate and having a contact hole, *e.g.*, 18a, in the drain electrode of the TFT; and (4) a pixel electrode, *e.g.*, 19a as discussed in paragraph [59] of the main body of the specification, made of a polycrystalline transparent conductive film of sufficient thickness to prevent generation of a galvanic effect by a stripper, and connected to the drain electrode through the contact hole, the drain electrode having a single-layer structure.

Claim 27 is directed to a pad structure of an LCD device, comprising (1) a substrate, *e.g.*, 11; (2) a metal film, *e.g.*, 12c, formed on the substrate and functioning as a pad for the LCD device; and (3) a polycrystalline transparent conductive film, *e.g.*, 19c as discussed in paragraph [59] of the main body of the specification, having a thickness sufficient to prevent generation of a galvanic effect by a stripper, and formed on the metal film, wherein the metal film is formed of a same material as a gate line or a data line.

Claim 28 is directed to a method for manufacturing an LCD device, comprising the steps of (1) forming a gate line including a gate electrode and a gate pad on a substrate; (2) forming a gate insulating film on an entire surface of the substrate; (3) forming a semiconductor film above the gate electrode; (4)

forming a data line including a data pad to form source and drain electrodes of a TFT at both sides above the semiconductor film; (5) forming a passivation film on the entire surface of the substrate; (6) forming contact holes in the drain electrode, the gate pad and the data pad of the TFT; and (7) forming, in each pixel region, polycrystalline transparent conductive films of sufficient thickness to prevent generation of a galvanic effect by a stripper, and connected to the drain electrode, the gate pad and the data pad through the contact holes, wherein at least one of the drain electrode, the gate pad and the data pad has a single-layer structure. Appellants respectfully direct the attention of the honorable Board members to Figs, 3A-3D and 4A-4D, which illustrate semiconductor device structures at different stages of the claimed method.

## **VI. GROUND OF REJECTION**

A. Claims 1, 18, 17 and 26-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,337,520 to Jeong et al. (hereinafter, "Jeong") in view of U.S. Patent 6,433,842 to Kaneko et al. (hereinafter, "Kaneko") and further in view of U.S. Patent 6,310,674 to Suzuki. This rejection is respectfully traversed.

In rejecting claims under 35 U.S.C. §103, it is incumbent on the Examiner to establish a factual basis to support the legal conclusion of obviousness. See, In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from

some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. Note, In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Eritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

A suggestion, teaching, or motivation to combine the prior art references is an “essential evidentiary component of an obviousness holding.” C.R. Bard, Inc. v. M3 Sys. Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998). This showing must be clear and particular, and broad conclusory statements about the teaching of multiple references, standing alone, are not “evidence.” See In re Dembiczak, 175 F.3d 994 at 1000, 50 USPQ2d 1614 at 1617 (Fed. Cir. 1999).

Jeong discloses an LCD structure having a drain line made of Molybdenum or a Molybdenum alloy – see col. 7, lines 16-30.



The Office Action admits that Jeong does not disclose a pixel electrode made of an amorphous transparent conductive film or a polycrystalline transparent conductive film for preventing a generation of a galvanic effect.

In an attempt to overcome these deficiencies in Jeong, the Office Action turns to Kaneko and Suzuki.

Kaneko, in col. 5, lines 34-65, discloses that, in the case where a layered structure is used for drain lines, a third conductive layer may be formed under the aluminum layer to secure contact with the underlying semiconductor layer, and, in that case, amorphous indium tin oxide (a-ITO) or indium zinc oxide (IZO) that allows for use of a weak-acid etchant is preferably used as the material of the pixel electrodes so that the aluminum alloy is prevented from being damaged during etching of the pixel electrodes. The damage addressed by Kaneko is explained as the second challenge to be solved by Kaneko. The desired result of the second challenge is that “the second conductive layer will not be etched away at the bottom inside of the contact hole securing connection with the pixel electrode” – see col. 3, lines 18-25, of Kaneko.

Appellants respectfully note that Kaneko does not mention occurrence of a galvanic effect to be overcome.

Furthermore, Appellants respectfully submit that this teaching of Kaneko is not relevant to, nor is obvious to apply to, Jeong because this teaching of Kaneko is limited to situations in which a third conductive layer is formed under an aluminum layer to secure contact with the underlying semiconductor layer. This type of situation is not present in Jeong. In this regard, reference is made to Fig. 10 of Jeong, in which the underlying semiconductor layer 520 is directly connected to drain electrode 620, and pixel electrode 800 is directly connected to drain electrode 620. Moreover, Kaneko has a layered drain

electrode (layers 21 and 22) whereas Jeong has a single layer electrode 620. In other words, the Kaneko's situation is not the same as the Jeong's situation. Nor does Jeong disclose any galvanic effect problems. Nor does Kaneko disclose galvanic effects, either explicitly or inherently (*i.e.*, necessarily). All that Kaneko discloses is corrosion of aluminum during etching resulting in etching away the second conductive layer, not, like in Appellants' case, of a stripper diffusing into the grain boundary of polycrystalline ITO during removal of the photoresist to generate a galvanic effect with the pad so that miniature gaps are formed at an interface between the pad contact film and the pad region causing contact failure.

In order to demonstrate inherent disclosure of a feature in a claim, the theory of inherency must be supported by facts and/or technical reasoning that reasonably support a determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. Ex parte Levy, 17 USPQ2d 1461 (BPAI 1990) (emphasis added). Moreover, in order for prior art to anticipate a claim . . . the inherency must be certain. Glaxo, Inc. v. Novopharm Ltd., (EDNC 1993) 830 F. Supp 871, 29 USPQ2d 1126; Ex parte Cyba (POBA 1966) 155 USPQ 756; Ex parte McQueen (POBA 1958) 123 USPQ 37. The fact that a prior art article may inherently have the characteristics of the claimed product is not sufficient. Ex parte Skinner (BPAI 1986) 2 USPQ2d 1788. Inherency must be a necessary result and not merely a possible result, *i.e.*, inherency may not be established by probabilities or possibilities. In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) and In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

In this regard, the Office Action fails to provide objective factual evidence that Kaneko discloses solving a galvanic effect problem, explicitly or inherently, or that one of ordinary skill in the art would be motivated to turn to Kaneko to

modify Jeong, which has neither disclosure of a galvanic effect problem nor the same electrode composition and structure as Kaneko.

In fact, as noted above, Jeong's drain line is made of Molybdenum or a Molybdenum alloy. However, Kaneko discloses using a dual layered drain electrode, where Cr layer 21 is the bottom layer and Mo layer 22 is the top layer. In col. 5, Kaneko discloses using amorphous ITO pixel electrodes with aluminum drain electrodes but using polycrystalline ITO pixel electrodes with molybdenum alloy drain electrodes (col. 5).

Moreover, because Jeong discloses a Mo or Mo alloy drain electrode, if Kaneko's teaching were followed, one would use polycrystalline ITO for pixel electrodes in Jeong, and would not use amorphous ITO pixel electrodes, as recited in claims 1 and 18.

Under such circumstances, the Office Action has not made out a *prima facie* showing that a skilled worker would be properly motivated to modify Jeong to provide amorphous ITO as the pixel electrode or to otherwise make out a *prima facie* case that the claimed invention is obvious based on Jeong and Kaneko.

On page 4 of the final Office Action, the Office Action states "[T]he galvanic effect means that the electrode generates galvanic corrosion during etching step, and that is a general available knowledge." Appellants' response to this general statement is that the Office Action does not show its relevance and applicability to Jeong, the main reference relied on in rejecting these claims, or to Kaneko as a matter of explicit or inherent disclosure, or to motivate one of ordinary skill in the art to modify Jeong, as suggested. Appellants respectfully submit that this general statement is nothing more than a broad conclusory statement about the teaching of no reference in

particular and, standing alone, is not “evidence” of proper motivation to modify Jeong, as suggested. Compare, In re Dembiczak, 175 F.3d 994 at 1000, 50 USPQ2d 1614 at 1617 (Fed. Cir. 1999).

The Office Action then turns to Suzuki, which discloses using amorphous ITO pixel electrodes instead of polycrystalline ITO pixel electrodes to permit the use of weak etching acids. Suzuki contains no disclosure of using the ITO pixel electrodes to reduce or eliminate a galvanic effect, and certainly does not teach varying thickness of the ITO layer in any manner whatsoever, let alone for reducing a galvanic effect. In fact, Suzuki discloses only a single thickness of 800 Angstroms for the ITO pixel electrode layer thickness. The disclosure of a single thickness ITO layer coupled with the complete failure to discuss galvanic effect problems is evidence of the complete failure of Suzuki to appreciate providing an ITO pixel electrode layer of sufficient thickness to prevent galvanic effects.

Moreover, because the base reference, Jeong, uses Mo or Mo alloy drain electrodes, and because Kaneko teaches not using amorphous ITO pixel electrodes in such a situation, one of ordinary skill in the art would not be motivated to turn to Suzuki to modify Jeong-Kaneko to provide amorphous ITO pixel electrodes in Jeong. In other words, one of ordinary skill in the art would not look to Suzuki to modify the Jeong-Kaneko reference combination because that reference combination teaches away from using amorphous ITO pixel electrodes with Jeong’s drain electrode materials.

Accordingly, Appellants respectfully submit that the Office Action fails to make out a *prima facie* case that it would not be obvious to modify Jeong-Kaneko in view of Suzuki to achieve the claimed invention because of the explicit teaching in Kaneko to use amorphous ITO pixel electrodes with Al or Al

alloy drain electrodes, and to use polycrystalline ITO pixel electrodes with Mo or Mo alloy drain electrodes.

Furthermore, with respect to claim 17, the burden of establishing the existence of a method of preventing a galvanic effect is even greater than the burden associated with establishing the existence of something being inherent in a device because it requires objective factual evidence of the performance of the claimed step being actually performed. Because none of the three applied references explicitly or inherently discloses or suggests the concept of preventing galvanic effects, it most certainly does not disclose or suggest a method for preventing a galvanic effect in general, let alone by providing a film of sufficient thickness to do so.

With respect to claims 26-28, none of the three references discloses varying the thickness of a polycrystalline transparent conductive film in general, or specifically a polycrystalline ITO pixel electrode to prevent generation of a galvanic effect in general, or caused by a stripper.

Reconsideration and withdrawal of this rejection of claims 1, 8, 17 and 26-28 is respectfully requested.

B. Claims 2-7, 9-12, 14-16, and 18-24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Jeong, Kaneko and Suzuki, applied as in the rejection of claims 1, 8, 17 and 26-28, and further in view of U.S. Patent 5,135,581 to Tran. This rejection is respectfully traversed.

With respect to claims 2-5, 9-12 and 18-22, Appellants respectfully submit that even if it were proper to modify the Jeong-Kaneko-Suzuki reference combination as suggested in view of Tran (which is not the case) that the resulting modified reference combination would not meet or render obvious the

claimed invention, at least for the reasons presented in the above traversal of the rejection of claims 1, 8, 17 and 26-28.

Furthermore, the alleged motivation to modify the improper base reference combination in view of Tran is given as “reducing visible light absorption and achieving more stable characteristics.” Unfortunately, the Office Action fails to provide objective evidence in the applied prior art of a need, or the knowledge of a need to “have reduced visible light absorption or more stable characteristics” in the claimed invention.

Thus, this reason is based completely on improper hindsight reconstruction of the claimed invention based solely on Appellants’ disclosure.

Moreover, “reducing visible light absorption and achieving more stable characteristics” is nothing more than a broad conclusory statement about the teaching of multiple references, and, standing alone, is not “evidence” of proper motivation to the base reference combination (which itself is improper). See In re Dembiczak, cited above.

Accordingly, Appellants respectfully submit that this rejection of claims 2-5, 9-12 and 18-22 is improper and should be withdrawn.

With respect to claims 6, 7, 15, 16, 23 and 24, the Office Action notes that Jeong discloses pixel electrode thicknesses of from 300 Angstroms to 2000 Angstroms, and that range is said to overlap the recited thickness range of from 500 to 2000 Angstroms. The Office Action fails to demonstrate that this thickness range of the polycrystalline ITO pixel electrode would inherently prevent galvanic effects. Something that is inherently disclosed must necessarily occur, not just possibly or probably, but necessarily. Under the doctrine of inherency, if an element is not expressly disclosed in a prior art

reference, the reference will still be deemed to anticipate a subsequent claim if the missing element “is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” Cont’l Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). “Inherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

Moreover, the Office Action must present objective factual evidence of this separate and apart from Appellants’ disclosure, which cannot properly be used against Appellants. See, In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

The Office Action fails to present any objective factual evidence to support a conclusion that Jeong-Kaneko-Suzuki inherently discloses the claimed invention.

Furthermore, with respect to method claims 18-24, the burden of establishing the existence of a method of preventing a galvanic effect is different than the burden associated with establishing the existence of something being inherent in a device. Because none of the three applied references discloses or suggests the concept of preventing galvanic effects, it most certainly does not disclose or suggest a method for preventing a galvanic effect in general, let alone by providing a film of sufficient thickness to do so.

With respect to claim 14, which is patentable at least for the reasons that claim 8, from which it depends, is patentable, Jeong does disclose a single layer metal pad. However, both Kaneko and Suzuki disclose double layer metal

pad structures. It is interesting how the Office Action selectively applies some teachings of Kaneko and Suzuki while deliberately not applying others, such as the advantages of a two-layer metal pad structure. This selective approach exemplifies the overall improper method of this Office Action applying the secondary and tertiary references to Jeong, the primary reference, in making these rejections. It is fundamentally improper for an Examiner to pick and choose only certain selected elements of one or more references while not applying other features of those same references.

Accordingly, reconsideration and reversal of this rejection of claims 6-7, 14-16 and 23-24 are respectfully requested.

## **VII. CLAIMS**

Appellants respectfully submit that claims 1-12, 14-24 and 26-28 are patentable over the applied art and that all of the rejections of record should be reversed. These claims are duplicated in Appendix A attached hereto.

## **IX. EVIDENCE**

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.



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**X. RELATED PROCEEDINGS APPENDIX**

No related proceedings are referenced in II above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: February 23, 2006

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Attachment

**APPENDIX A - CLAIMS**

1. (Previously Presented) An LCD device comprising:

a substrate;

a TFT having a gate electrode and source/drain electrodes on the substrate;

a passivation film formed on an entire surface of the substrate and having a contact hole in the drain electrode of the TFT; and

a pixel electrode made of an amorphous transparent conductive film of sufficient thickness to prevent a generation of a galvanic effect, and connected to the drain electrode through the contact hole, the drain electrode having a single-layer structure.

2. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode is formed of ITO in which H<sub>2</sub>O is added.

3. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode is formed of ITO in which H<sub>2</sub> is added.

4. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode is formed of ITO produced at a predetermined temperature.

5. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode is formed of any one of amorphous IZO and amorphous ITZO.

6. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode has a thickness of approximately 500Å to 2000Å.

7. (Original) The LCD device as claimed in claim 1, wherein the pixel electrode is formed of a polycrystal transparent conductive film having a thickness of above 500Å to 2500Å.

8. (Previously Presented) A pad structure of an LCD device, comprising:

a substrate:

a metal film formed on the substrate and functioning as a pad for the LCD device; and

an amorphous transparent conductive film of sufficient thickness to prevent a generation of a galvanic effect, and formed on the metal film,

wherein the metal film is formed of a same material as a gate line or a data line.

9. (Original) The pad structure as claimed in claim 8, wherein the amorphous transparent conductive film is formed of ITO in which H<sub>2</sub>O is added.

10. (Original) The pad structure as claimed in claim 8, wherein the amorphous transparent conductive film is formed of ITO in which H<sub>2</sub> is added.

11. (Original) The pad structure as claimed in claim 8, wherein the amorphous transparent conductive film is formed of ITO produced at a predetermined temperature.

12. (Original) The pad structure as claimed in claim 8, wherein the amorphous transparent conductive film is formed of any one of amorphous IZO and amorphous ITZO.

13. (Canceled)

14. (Previously Presented) The pad structure as claimed in claim 8, wherein the metal film has a single-layer structure.

15. (Original) The pad structure as claimed in claim 8, wherein the amorphous transparent conductive film has a thickness of approximately 500Å and 2000Å.

16. (Original) The pad structure as claimed in claim 8, wherein a polycrystal transparent conductive film having a thickness of above 500Å to 2500Å is formed instead of the amorphous transparent conductive film.

17. (Previously Presented) A method for manufacturing an LCD device, comprising the steps of:

forming a gate line including a gate electrode and a gate pad on a substrate;

forming a gate insulating film on an entire surface of the substrate;

forming a semiconductor film above the gate electrode;

forming a data line including a data pad to form source and drain electrodes of a TFT at both sides above the semiconductor film;

forming a passivation film on the entire surface of the substrate;

forming contact holes in the drain electrode, the gate pad and the data pad of the TFT; and

forming, in each pixel region, amorphous transparent conductive films of sufficient thickness to prevent a generation of a galvanic effect,

and connected to the drain electrode, the gate pad and the data pad through the contact holes,

wherein at least one of the drain electrode, the gate pad and the data pad has a single-layer structure.

18. (Previously Presented) The method as claimed in claim 17, wherein at least one of the amorphous transparent conductive films is formed of ITO in which H<sub>2</sub>O is added.

19. (Original) The method as claimed in claim 17, wherein at least one of the amorphous transparent conductive films is formed of ITO in which H<sub>2</sub> is added.

20. (Original) The method as claimed in claim 17, wherein at least one of the amorphous transparent conductive films is formed of ITO produced at a predetermined temperature.

21. (Original) The method as claimed in claim 17, wherein at least one of the amorphous transparent conductive films is formed of any one of amorphous IZO and amorphous ITZO.

22. (Original) The method as claimed in claim 17, further comprising the step of:

performing a thermal process to at least one of the amorphous transparent conductive films at a temperature of around 150° to 350°.

23. (Original) The method as claimed in claim 17, wherein at least one of the amorphous transparent conductive films is formed at a thickness of approximately 500Å to 2000Å.

24. (Original) The method as claimed in claim 17, wherein a polycrystal transparent conductive film having a thickness of above 500Å and 2500Å is formed instead of at least one of the amorphous transparent conductive films.

25. (Canceled)

26. (Previously Presented) An LCD device comprising:

a substrate;

a TFT having a gate electrode and source/drain electrodes on the substrate;

a passivation film formed on an entire surface of the substrate and having a contact hole in the drain electrode of the TFT; and

a pixel electrode made of a polycrystalline transparent conductive film of sufficient thickness to prevent generation of a galvanic effect by a stripper, and connected to the drain electrode through the contact hole, the drain electrode having a single-layer structure.

27. (Previously Presented) A pad structure of an LCD device, comprising:

a substrate;

a metal film formed on the substrate and functioning as a pad for the LCD device; and

a polycrystalline transparent conductive film having a thickness sufficient to prevent generation of a galvanic effect by a stripper, and formed on the metal film,

wherein the metal film is formed of a same material as a gate line or a data line.

28. (Previously Presented) A method for manufacturing an LCD device, comprising the steps of:

forming a gate line including a gate electrode and a gate pad on a substrate;

forming a gate insulating film on an entire surface of the substrate;

forming a semiconductor film above the gate electrode;



forming a data line including a data pad to form source and drain electrodes of a TFT at both sides above the semiconductor film;

forming a passivation film on the entire surface of the substrate;

forming contact holes in the drain electrode, the gate pad and the data pad of the TFT; and

forming, in each pixel region, polycrystalline transparent conductive films of sufficient thickness to prevent generation of a galvanic effect by a stripper, and connected to the drain electrode, the gate pad and the data pad through the contact holes,

wherein at least one of the drain electrode, the gate pad and the data pad has a single-layer structure.